Introduction

EScala is a design platform that accelerates the implementation of complex, compute intensive algorithms in SoC/ASSP/FPGA. It targets low power deeply embedded applications with high performance and bandwidth requirements, conventionally reserved to fixed function logic implemented with RTL. EScala uses C/C++ as a design entry language and automatically generates application specific cores and allows to optimize and scale the generated core to best fit the application's area, low power and performance profile.

Features

Highly scalable programmable core framework:
- Multicore data-flow architecture with simple programming model
- Configuration can be user or application driven (semi-automated).
- Up to 32 computational slots
- Configurable number of load/store units (1-32)
- Configurable number of input/output memory channels accessible from any slot
- Number of registers tunable to application needs
- Common register file accessible from all slots

Optional Features

- User defined Extension Instructions (EI) that augment the basic instruction set
- In System Debug module accessible through JTAG port
- Dual/Quad SIMD instructions
- Programmable interrupt controller
- Program memory compression
- EScalaLib application specific extension instruction (EI) library
- Programmable address generation units

Applications

- High bandwidth data intensive algorithms like 3D and HD audio, audio CODECs, speech recognition and video
- Replacement for fixed function high-performance blocks, where programmability is a plus
- Low power / low gate count system controllers
- Rapid algorithm FPGA prototyping
- High frequency trading FPGA applications
- Low latency computing applications
- Complex control applications

Tools

- C/C++ compiler / assembler / debugger
- EScala's Instruction Set Simulator
- EScala's Stream Optimizer
- Advanced VLIW instruction scheduling
- Instruction set analysis / customization
- Automated complex instruction generation
- Instruction encoding optimization
- Configuration parameter scanning
- Miscellaneous optimization steps
Deliverables

- Synthesizable Verilog/VHDL RTL source
- Simulation scripts
- Self-checking test environment
- Test-bench
- Sanity regression
- ASIC and FPGA Synthesis scripts
- User documentation
- Complete SW toolset for Linux and Windows
- Gnu compiler / assembler / linker
- EScala optimizer
- EScala Instruction Set Simulator

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About Esencia

Esencia Technologies, Inc. provides IP cores and design services for the semiconductor industry. We can assist the core generation process to build the best fitting core for your application.